ABSTRACT

A processor includes an instruction decoder to decode instructions into micro-operations for execution. The instruction decoder may include a programmable logic array to store templates to be addressed by instructions during decoding of the instructions. A collapsed template is addressed by one or more instructions during decoding into fused micro-operations and by one or more instructions during decoding into simple micro-operations. The instruction decoder may also include a multiplexer to select values of a field of the micro-operation based at least on an indication that the instruction being decoded is not being decoded into a simple micro-operation. The instruction decoder may also include a multiplexer to select values of a field of the micro-operation based at least on bits of a template field, where the number of bits of the template field is less than the number of bits of the field of the micro-operation.